WHAT IS CLAIMED IS:

1. A method of designing a packaged integrated circuit, including a package substrate and an integrated circuit, the method comprising the steps of:

designing the integrated circuit with a plurality of integrated circuit standardized functional blocks, where each of the plurality of integrated circuit standardized functional blocks has a known function and a known integrated circuit contact array pattern, and the integrated circuit is designed by selecting desired ones of the integrated circuit standardized functional blocks according to functions desired for the integrated circuit, and

designing the package substrate with a plurality of package substrate standardized functional blocks, where each of the plurality of package substrate standardized functional blocks has a known package substrate contact array pattern, a known signal trace routing layer pattern, a known ground plane layer pattern, and a known power plane layer pattern,

where a given one of each of the plurality of package substrate standardized functional blocks is associated with a given one of the plurality of integrated circuit standardized functional blocks, and the package substrate is designed by selecting package substrate standardized functional blocks associated with the desired ones of the integrated circuit standardized functional blocks.

2. The method of claim 1 wherein the known signal trace routing layer pattern comprises patterns for a plurality of known signal trace routing layers.

3. The method of claim 1 wherein the known ground plane routing layer pattern comprises patterns for a plurality of known ground plane routing layers.

4. The method of claim 1 wherein the known power plane routing layer pattern comprises patterns for a plurality of known power plane routing layers.

5. The method of claim 1 wherein the given one of each of the plurality of package substrate standardized functional blocks that is associated with the given one of the plurality of integrated circuit standardized functional blocks are aligned so as to meet between the integrated circuit and the package substrate.

6. The method of claim 1 wherein the package substrate contact array pattern of the given one of each of the plurality of package substrate standardized functional blocks that is associated with the integrated circuit contact array pattern of the given one of the plurality of integrated circuit standardized functional blocks are aligned so as to meet between the integrated circuit and the package substrate.

7. A method of designing a package substrate for a packaged integrated circuit, including the package substrate and an integrated circuit having a plurality of integrated circuit standardized functional blocks, where each of the plurality of integrated circuit standardized functional blocks has a known function and a known integrated circuit contact array pattern, the method comprising the steps of:

designing the package substrate with a plurality of package substrate standardized functional blocks, where each of the plurality of package substrate standardized functional blocks has a known package substrate contact array pattern, a known signal trace routing layer pattern, a known ground plane layer pattern, and a known power plane layer pattern,

where a given one of each of the plurality of package substrate standardized functional blocks is associated with a given one of the plurality of integrated circuit standardized functional blocks, and the package substrate is designed by selecting package substrate standardized functional blocks associated with the integrated circuit standardized functional blocks.

8. The method of claim 7 wherein the known signal trace routing layer pattern comprises patterns for a plurality of known signal trace routing layers.

9. The method of claim 7 wherein the known ground plane routing layer pattern comprises patterns for a plurality of known ground plane routing layers.

10. The method of claim 7 wherein the known power plane routing layer pattern comprises patterns for a plurality of known power plane routing layers.

11. The method of claim 7 wherein the given one of each of the plurality of package substrate standardized functional blocks that is associated with the given one of the plurality of integrated circuit standardized functional blocks are aligned so as to meet between the integrated circuit and the package substrate.

12. The method of claim 7 wherein the package substrate contact array pattern of the given one of each of the plurality of package substrate standardized functional blocks that is associated with the integrated circuit contact array pattern of the given one of the plurality of integrated circuit standardized functional blocks are aligned so as to meet between the integrated circuit and the package substrate.

13. A method of designing a first electronic structure for a unified circuit structure, including the first electronic structure and a second electronic structure having a plurality of second standardized functional blocks, where each of the plurality of second functional blocks has a known function and a known second contact array pattern, the method comprising the steps of:

designing the first electronic structure with a plurality of first standardized functional blocks, where each of the plurality of first standardized functional blocks has a known first contact array pattern, a known signal trace routing layer pattern, a known ground plane layer pattern, and a known power plane layer pattern,

where a given one of each of the plurality of first standardized functional blocks is associated with a given one of the plurality of second functional blocks, and the first electronic structure is designed by selecting first standardized functional blocks associated with the second functional blocks.

14. The method of claim 13 wherein the known signal trace routing layer pattern comprises patterns for a plurality of known signal trace routing layers.

15. The method of claim 13 wherein the known ground plane routing layer pattern comprises patterns for a plurality of known ground plane routing layers.

16. The method of claim 13 wherein the known power plane routing layer pattern comprises patterns for a plurality of known power plane routing layers.

17. The method of claim 13 wherein the given one of each of the plurality of first standardized functional blocks that is associated with the given one of the plurality of second functional blocks are aligned so as to meet between the first electronic structure and the second electronic structure.

18. The method of claim 13 wherein the first contact array pattern of the given one of each of the plurality of first standardized functional blocks that is associated with the second contact array pattern of the given one of the plurality of second standardized functional blocks are aligned so as to meet between the first electronic structure and the second electronic structure.

19. The method of claim 13 wherein the first electronic structure is a package substrate, the second electronic structure is an integrated circuit, and the unified electronic structure is a packaged integrated circuit.

20. The method of claim 13 wherein the first electronic structure is a packaged integrated circuit and the second electronic structure is printed circuit board.